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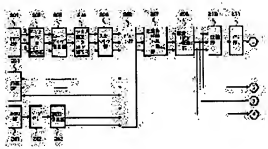
(54) PICTURE PROCESSOR, PICTURE PROCESSING METHOD AND NETWORK SYSTEM

(57)Abstract:

PURPOSE: To provide a picture processor or the like capable of using a common encoding means and reducing a memory size in spite of whether inputted picture data are encoded or not.

CONSTITUTION: An input masking part 206 outputs picture data for which an original is read front a CCD sensor 201. In the meantime, a JPEG-I/F 241 inputs JPEG data by ATM and the inputted JPEG data are tentatively stored in a page memory 242, then read from the page memory 242 in synchronism with a picture formation timing and decoded in a JPEG expansion part 243. A bus selector 232 selects the picture data outputted from the input masking part 206 or the JPEG expansion part 243 and the selected picture data are sent through a color space conversion part 207 and a variable magnification part 208 to a compression part 210.



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• NOTICES •

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] First input means to input the encoded image data, and a decode means to decode the encoded image data which was inputted by said first input means, A selection means to choose the image data inputted by the second input means which inputs the image data which is not encoded, and the image data decoded by said decode means or said second input means, The image processing system characterized by having a storage means to encode and memorize the image data chosen by said selection means, and an output means to decode and output the encoded image data which was memorized by said storage means.
[Claim 2] First input means to input the encoded image data, and the first storage means which memorizes a part or all of image data that was inputted by said first input means, and that was encoded, A decode means to decode the encoded image data which was memorized by said first storage means, A selection means to choose the image data inputted by the second input means which inputs the image data which is not encoded, and the image data decoded by said decode means or said second input means, The image processing system characterized by having the second storage means which encodes and memorizes the image data chosen by said selection means, and an output means to decode and output the encoded image data which was memorized by said second storage means.
[Claim 3] Furthermore, it is the image processing system which was equipped with the control means which controls the R/W timing of said first storage means, and two or more image formation means to form an image based on the image data outputted by said output means, and was indicated by claim 2 characterized by said control means reading image data from said first storage means synchronizing with the image formation timing of said image formation means.
[Claim 4] It is the image processing system which said image processing system was connected to the network system, and was indicated by any of claim 1 to claim 3 characterized by said first input means inputting the encoded image data to which said network is asynchronous-transmitted they are.
[Claim 5] Said network is the image processing system indicated by claim 4 characterized by being the ATM network to which data are transmitted by ATM (Asynchronous Transfer Mode).
[Claim 6] Said network is the image processing system indicated by claim 4 characterized by being a Local Area Network (LAN).
[Claim 7] Said encoded image data is the image processing system indicated by any of claim 1 to claim 6 characterized by encoding by the JPEG method they are.
[Claim 8] Said encoded image data is the image processing system indicated by any of claim 1 to claim 6 characterized by encoding by the MPEG method they are.
[Claim 9] Said selection means is the image processing system indicated by any of claim 1 to claim 3 characterized by choosing which image data from the said first or second [said] input means based on the condition of the signal beforehand sent to ********** and abbreviation coincidence again,

a command, or a hardware key.
[Claim 10] Said selection means is the image processing system indicated by claim 9 characterized by forbidding the image entry of data by said second input means while having inputted image data from said first input means.
[Claim 11] Said selection means is the image processing system indicated by claim 9 characterized by forbidding the image entry of data by said first input means while having inputted image data from said second input means.
[Claim 12] The image data inputted by said second input means is the image processing system indicated by any of claim 1 to claim 11 characterized by being what reads a manuscript and obtained they are.
[Claim 13] The network system characterized by connecting said image processing system indicated by any of claim 1 to claim 12 they are.
[Claim 14] The first input step which inputs the encoded image data, and the decode step which decodes the encoded image data which was inputted at said first input step, The selection step which chooses the image data inputted at the second input step which inputs the image data which is not encoded, and the image data decoded at said decode step or said second input step, The image-processing approach characterized by having the coding step which encodes the image data chosen at said selection step, and a storage means is made to memorize, and the output step which decodes and outputs the encoded image data which was memorized by said storage means.
[Claim 15] The first input step which the encoded image data is inputted [first] and makes the first storage means memorize the part or all, The decode step which decodes the encoded image data which was memorized for said first storage means, The selection step which chooses the image data inputted at the second input step which inputs the image data which is not encoded, and the image data decoded at said decode step or said second input step, The image-processing approach characterized by having the coding step which encodes the image data chosen at said selection step, and the second storage means is made to memorize, and the output step which decodes and outputs the encoded image data which was memorized by said second storage means.
[Claim 16] Said first input step is the image-processing approach indicated by claim 14 or claim 15 characterized by inputting the encoded image data to which a network is asynchronous-transmitted.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the image processing system which processes and outputs the inputted image data, the image-processing approach, and the network system which connected the image processing system, concerning an image processing system, the image-processing approach, and a network system.
[0002]
[Description of the Prior Art] The image data whose color was separated is treated, it connects with the Local Area Network (henceforth "LAN") using the ATM network transmitted by ATM (Asynchronous Transfer Mode), or the Ethernet which transmits data in the modes other than ATM, and the interface of an image processing system transmits or outputs the image data encoded by coding methods, such as JPEG and MPEG. However, a limping gait, such as changing and outputting the image data itself whose color was separated, and the data which encoded them, is not.
[0003]
[Problem(s) to be Solved by the Invention] However, there were the following troubles in the above-mentioned conventional example. The image processing system itself needs to output image data with constant speed. In the equipment especially equipped with two or more image formation means, unless image data is outputted with constant speed from an image-processing means, an image cannot be formed. That is, when there are image data which read the manuscript image by which a synchronous input is carried out, and image data to which variable length coding inputted through an ATM network, such as JPEG and MPEG, was given, an image processing system must output both image data with constant speed.
[0004] Furthermore, in the image processing system equipped with the image memory, in order to reduce the memory size, the approach of compressing into the image memorized to an image memory is taken. However, the image processing system which performs such picture compression is not taken into consideration to being used combining a network system which was mentioned above.
[0005] This invention aims at offering the image processing system, the image-processing approach, and network system for solving an above-mentioned problem which can reduce memory size using a coding means common irrespective of the image data which it is and was inputted.
[0006]
[Means for Solving the Problem] It reaches. [Function] This invention is equipped with the following configurations as a way stage which attains the aforementioned object.
[0007] The image processing system concerning this invention is first input means to input the encoded image data, A decode means to decode the encoded image data which was inputted by said first input means, A selection means to choose the image data inputted by the second input means

which inputs the image data which is not encoded, and the image data decoded by said decode means or said second input means, The image processing system characterized by having a storage means to encode and memorize the image data chosen by said selection means, and an output means to decode and output the image data memorized by said storage means.

[0008] The image-processing approach concerning this invention is first input step which inputs the encoded image data, The decode step which decodes the encoded image data which was inputted at said first input step, The selection step which chooses the image data inputted at the second input step which inputs the image data which is not encoded, and the image data decoded at said decode step or said second input step, It is characterized by having the coding step which encodes the image data chosen at said selection step, and a storage means is made to memorize, and the output step which decodes and outputs the image data memorized by said storage means.

[0009] The network system concerning this invention is first input means to input the encoded image data, A decode means to decode the encoded image data which was inputted by said first input means, A selection means to choose the image data inputted by the second input means which inputs the image data which is not encoded, and the image data decoded by said decode means or said second input means, It is characterized by connecting the image processing system equipped with a storage means to encode and memorize the image data chosen by said selection means, and an output means to decode and output the image data memorized by said storage means.

[0010]

[Example] Hereafter, the image processing system of one example concerning this invention is explained to a detail with reference to a drawing. Although the example which applies this invention to the image processing system of a color copying machine is explained below, this invention may be what kind of thing, as long as not only this but the image data by which variable length coding was carried out is equipment with which it can apply to all the image processing systems inputted by ATM, and the output destination change also forms not only a color copying machine but an image.

[0011]

[The 1st example]

[Structure-of-a-system] drawing 1 is the block diagram showing the example of a configuration of the network system of one example concerning this invention.

[0012] In drawing 1, 1101 is an ATM network and transmits various kinds of code data, such as image data encoded by coding methods, such as JPEG and MPEG, by ATM. 1103 is LAN, for example, transmits data in the modes other than ATM using Ethernet.

[0013] 1105 is facsimile apparatus, and it connects with the ATM network 1101 and it has compression / expanding function of image data. 1107 is a color printer, and it connects with the ATM network 1101 and it forms a color picture in the interior based on the image data which has page memory and elongated the code data which received.

[0014] 1109 and 1119 are the color copying machines equipped with the reader and the printer, respectively, and include the expanding circuit which elongates the compression image data written in the compression circuit which compresses the image data of the manuscript read by the reader for example, by the JPEG method, the page memory which writes in the compressed image data, and page memory, and is supplied to a printer. In addition, a color copying machine 1109 is connected to the ATM network 1101, and the color copying machine 1119 is connected to the server 1117 mentioned later. 1111 and 1117 are servers, respectively and a server 1111 once stores the image data inputted through the ATM network 1101. Moreover, the server 1117 is connected to the color copying machine 1119.

[0015] 1113 is a workstation and is for outputting and inputting image data to a server 1111. It is a personal computer, it connects with the ATM network 1101 and LAN1103, and 1115 performs various kinds of processings including edit of various image data while it delivers and receives code data, such

as MPEG and JPEG, by the meantime and performs coding and decode of data. Moreover, this personal computer 1115 is connected with the printer 1107 through the ATM network 1101 or the dedicated line.

[0016] 1121 is a digital television, it receives code data, such as MPEG and JPEG, through the ATM network 1101, decodes this, and displays it on a CRT display as a visible image. In addition, the thing using the ferroelectric liquid crystal called FLC may be used for this display. It is VTR, 1123 receives code data, such as MPEG and JPEG, through the ATM network 1101, and after it performs predetermined signal processing, such as remaining as it is or decode, it records the code data which received on a magnetic tape. Moreover, VTR1123 has the image data compression machine for recording on a magnetic tape, after having compressed the incompressible image data which received from the outside by MPEG or the JPEG method.

[0017] 1127 is a CATV station and sends out the image data compressed by MPEG or the JPEG method to the ATM network 1101. That is, the CATV station 1127 broadcasts an image through the ATN network 1101. 1129 and 1131 are routers, respectively, and a router 1129 connects the ATM network 1101 and other ATM networks, and they connect LAN of the ATM network 1101 and others. [router / 1131]

[0018] Moreover, the ATM network switch which is not illustrated is formed between facsimile apparatus 1105, the color printer 1107 and the color copying machine 1109, and the ATM network 1101.

[0019] JPEG data are explained among [JPEG coding], next the various data transmitted in the above-mentioned system. A JPEG coding method is an international-standards method aiming at compressing a color still picture using the frequency characteristics of image data, or human being's vision property.

[0020] Drawing 2 A is drawing showing the configuration of JPEG data, and code data and various marker codes are constituted as a layered structure of an image / frame / scan. That is, in the case of the data with which hierarchy coding of the frame was carried out, JPEG data consist of a SOI (Start Of Image) code, a frame, and an EOI (End Of Image) code, and it consists of two or more frames for every hierarchy, and when that is not right, it consists of single frames. Furthermore, a frame consists of a SOF (Start Of Frame) code, a frame header, and a scan, and the scan consists of an SOS (Start Of Scan) code, a scanning header, and code data. In addition, the above-mentioned scan consists of two or more scans, when dividing brightness data (Y) and two color difference data (Cr, Cb) and encoding (non interleave), and when encoding, without dividing each data (interleave), it consists of single scans.

[0021] Drawing and drawing 4 drawing 3 explains the coding algorithm in a JPEG base-line system to be are drawing explaining the decode algorithm in this system.

[0022] In drawing 3, the inputted image data is divided into a 8x8-pixel block in the blocking circuit 1201, and is changed into the spatial-frequency component (DCT multiplier) which consists of a dc component (DC) of a piece, and 63 alternating current components (AC) by carrying out 2-dimensional DCT (discrete cosine transform) of this in the DCT circuit 1202. Each obtained frequency component is **(ed) and quantized by the predetermined quantization multiplier in a quantizer 1203, respectively. After each quantized frequency component is divided into a dc component and an alternating current component, it is encoded by different algorithm, respectively. In addition, the multiplier from which a quantization multiplier generally differs for every frequency component is used, and the quantization multiplier to an important low-pass component is small set up compared with the quantization multiplier to a high-frequency component on vision. A high-frequency component with a low significance will be visually omitted by this, and data size will be reduced.

[0023] The separated dc component is inputted into a difference circuit 1204, and in order to use that correlation with an adjoining block is high, it is changed into the dc component and difference of a

precedence block. The obtained difference is inputted into the Huffman-coding machine 1205, and single dimension Huffman coding is carried out, and it serves as code data of a dc component.
[0024] On the other hand, an alternating current component is inputted into the scanning circuit 1206, visually, one by one, the jig ZAKUSU can of the 63 alternating current components is carried out, and they become the array of a single dimension from a frequency component low-pass [important]. The alternating current component put in order by the array of a single dimension is inputted into the judgment machine 207, and it is judged whether the value of each component is zero or they are values other than zero (effectiveness factor). A counter 1208 counts the run length of zero and the grouping circuit 1209 carries out grouping of the effectiveness factor with the value. Thus, the combination of the run length and group value which were acquired is inputted into the Huffman-coding machine 1210, and 2-dimensional Huffman coding is carried out, and it serves as code data of an alternating current component.
[0025] here -- the Huffman-coding machines 1205 and 1210 -- difference with an occurrence probability high about a dc component -- data size is reduced by assigning the shorter code length about the combination of the high run length and high effectiveness factor of an occurrence probability about a value and an alternating current component. Moreover, about what has a low occurrence probability, all patterns can be expressed with the number of codes of finite by combining with a predetermined code (ZRL code).
[0026] Although coding of the color static image of one sheet will be completed if the above processing is carried out to each block unit, after that, in the addition circuit 1211, the marker code mentioned above is added and each code data turns into JPEG data shown in drawing 2 A. In addition, since a quantization multiplier and Huffman coding can be set as arbitration, they add the quantization multiplier table and the Huffman table which were used for coding after the SOI code.
[0027] Next, the decode algorithmic language of JPEG is explained.
[0028] The inputted JPEG data are decoded in a decoder 1212 based on the attached Huffman table. The decoded dc component is added with the dc component of a precedence block in an adder 1213, the decoded alternating current component is rearranged in the sort circuit 1214, and each of that frequency component returns to the original two-dimensional array. Then, in the reverse quantizer 1215, Reverse DCT is performed in the IDCT circuit 1216, and each frequency component is returned to image data (decode data), after reverse quantization is carried out based on the attached quantization multiplier table.
[0029] If the above processing is performed in each block unit, decode of the color static image of one sheet will be completed.
[0030] In addition, when the EKUSUTENDO system which took in further various kinds of hierarchy coding is also accepted and it performs hierarchy coding, the SOF code is to express the class, although the JPEG method of the above algorithmic language is fundamental.
[0031] MPEG data are explained among [MPEG coding], next the various data transmitted in the above-mentioned system. Although an MPEG coding method is international standards aiming at carrying out high efficiency coding of the dynamic image and uses the frequency characteristics of image data, and human being's vision property like a JPEG method, it performs high efficiency coding using the redundancy of the direction of a time-axis still more peculiar to a dynamic image.
[0032] Although an MPEG method has MPEG1 which set the transfer rate to a maximum of 1.5 Mbps (es) for digital recording media, and MPEG 2 which meant abolishing the upper limit of a transmission rate and using by all transmission systems, such as a bidirectional digital multimedia device, for example, a digital video tape recorder, ATV (advanced television), and an optical fiber network, since the fundamental algorithm is almost the same, the DS and coding / decode algorithm are explained by using MPEG1 as the base. In addition, although two or more profiles (the simple profile and Maine profile, scalable one, space scalable, yes) have prescribed the usable coding approach in MPEG 2,

the typical Maine profile is the same as that of MPEG1 almost fundamentally.
[0033] First, the principle of the low bit rate coding method in MPEG is explained. the difference which the redundancy of time amount shaft orientations was reduced and was obtained because this coding method takes inter-frame difference -- high efficiency coding is realized for data DCT and by carrying out variable length coding and reducing the redundancy of the direction of space. That is, in the case of an animation, since correlation of a continuous frame is high, the redundancy of the direction of a time-axis can be reduced by taking in time difference with precedence or the frame which carries out backward to the frame which it is going to encode.
[0034] Then, as shown in drawing 5, the frame structure of an MPEG method consists of I-picture, a P-picture, and a B-picture, and combines these in predetermined sequence. the intra which encodes I-picture in the coding (intra-coded) mode in a frame here -- it is a coded image. P-picture is a predicting-coding (predictive coded) image which encodes difference with the frame (henceforth a "before frame") to precede, and B-picture is a both-directions predicting-coding (bi-directionally predictive coded) image which encodes the smallest difference among the difference between the interpolation images from a before frame, the frame (henceforth a "after frame") which carries out backward, or an order frame. In addition, when a new body appears in a frame, the difference may become small [direction] having taken difference with an after frame, and, as for both-directions predicting coding, this is taken into consideration rather than it takes difference with a before frame.
[0035] MPEG recommends the combination which makes such an I-picture, P-picture, and B-picture one unit (GOP: Group of Picture) by one sheet, four sheets, and ten sheets, respectively, allots I-picture to a head, and repeats and allots B-picture of two sheets, and P-picture of one sheet. Arranging I-picture for every fixed period aims at prevention of error propagation while making possible special playback of reverse playback etc., and partial regeneration which makes GOP a unit.
[0036] Next, the motion compensation of MPEG is explained.
[0037] Difference with the macro block near [where before or an after frame corresponds] the block is taken by making into a unit the macro block which collected [data / brightness] 2 blocks of 8x8-pixel blocks about 4 blocks and color difference data, by searching for the macro block with few differences, a motion vector is detected in the case of coding, and it encodes this motion vector as data. In the case of decode, the macro block data with which before or an after frame corresponds is extracted using a motion vector, and it decodes the code data encoded by this using the motion compensation. Once encoding a before frame on the occasion of such a motion compensation, again, it decodes, and considers as a before frame, and the macro block in a before [this] frame and the macro block of the frame which it is going to encode are used. In addition, although MPEG1 performs an inter-frame motion compensation, MPEG 2 performs the motion compensation between the fields. moreover, the difference obtained by the motion compensation -- data and a motion vector are encoded by DCT and Huffman coding which were explained previously.
[0038] Next, the DS of an MPEG method is explained.
[0039] Drawing 6 is drawing showing the DS of MPEG, and is a layered structure which consists of a video sequence layer, a GOP layer, a picture layer, a slice layer, a macro block layer, and a block layer. Hereafter, each class is explained sequentially from the bottom.
[0040] A block layer is constituted considering the block of 8x8 pixels as a unit for every brightness data and color difference data like JPEG, and DCT is performed for every unit of this.
[0041] A macro block layer attaches a macro block header by making into a unit what packed [data / brightness] 1 block of 8x8-pixel blocks at a time about 4 blocks and color difference data. As mentioned above, a motion compensation and coding are performed considering this macro block as a unit. The macro block header contains each data of the motion compensation of the macro block, and a quantization step, and the data showing whether six DCT blocks in a macro block (Y0, Y1, Y2, Y3, Cr, Cb) have data.

[0042] A slice layer consists of one or more macro blocks which stand in a row in order of the scan of an image, and a slice header. Since the quantization step of a slice header is used when it has data about the quantization step in the slice layer and each macro block does not have quantization step data of a proper, a slice header can make regularity the quantization step in a series of macro blocks in the same slice layer. in addition, the macro block of the head of a slice layer -- the difference of a dc component -- a value is reset.

[0043] A picture layer collects slice layers per frame, and consists of a header containing a picture start code etc., and one or more slice layers following this. In addition, the header of a picture layer contains the code which shows the coding mode of an image, the code which shows the precision (are they a pixel unit or a half-pixel unit?) of motion detection.

[0044] A GOP layer consists of the header containing a group start code, the time code which shows the time amount from initiation of a sequence, and two or more I following this, B frames, and P frames.

[0045] A video sequence layer begins from a sequence start code, and is ended by the sequence end code, and control data, image size, etc. required for decode, such as image size and an aspect ratio, and two or more GOP(s) are arranged between them.

[0046] As for the MPEG data with such structure, the bit stream is specified.

[0047] Next, the fundamental coding equipment and decode equipment treating MPEG data are explained.

[0048] Drawing 7 is the block diagram showing the example of a configuration of MPEG coding equipment, and is the image size for coding, As shown in drawing 9, there are an image (it corresponds to the Maine level in MPEG 2) corresponding to CCIR.601 of 1,920x1,080 pixels High (high-level response in MPEG 2) and 1,440x1,080-pixel High 1440 (yes, 1440 level in MPEG 2 response), 4:2:2, or 4:2:0 and SIF and CIF, and an image corresponding to a QCIF format, and it is aimed at the image size of a SIF format in the low level of MPEG1 and MPEG 2.

[0049] In drawing 7, 1301 is a blocking circuit and divides the inputted image data into a 8x8-pixel block. 1302 is a DCT circuit and gives DCT to the block inputted through the switch 1310. The inputted image data is switched according to I-picture or the other picture, in the case of I-picture, Contact a is chosen, and a switch 1310 chooses Contact b, when other. Therefore, in the case of I-picture, the block outputted from the blocking circuit 1301 is inputted into the DCT circuit 1302. Moreover, in other than I-picture, the motion compensation explained previously is performed.

[0050] 1303 is a quantizer and quantizes the DCT multiplier outputted from the DCT circuit 1302. 1304 is a variable-length encoder (henceforth "VLC"), and encodes the quantization multiplier outputted from the quantizer 1303. 1309 is a buffer and memorizes the sign outputted from VLC temporarily. In addition, although VLC1304 performs 2-dimensional Huffman coding like JPEG, they differ at the point which assigns a predetermined code (escape code) uniquely about what has a low occurrence probability.

[0051] 1308 is a local decoder, consists of a reverse quantizer 1311 and a reverse DCT circuit 1312, and performs reverse quantization and Reverse DCT to the quantization multiplier outputted from the quantizer 1303. 1306 is a motion vector detector, inputs the block outputted from the local decoder 1308 through the adder 1313, and the block outputted from the blocking circuit 1301, and detects a motion vector. 1305 is a motion compensation circuit, and it outputs the response macro block in a predetermined frame (a before frame, after frames, or these interpolation frames) with reference to the motion vector detected in the motion vector detector 1306 while it inputs the block outputted from the local decoder 1308 through the adder 1313. In addition, the motion vector detector 1306 performs the comparison with the frame to be encoded from now on and a reference frame, a motion vector is obtained, and the detection result specifies the macro block which the motion compensation circuit 1305 should output. Moreover, 1314 is a switch which is closed in other than I-picture.

[0052] 1316 is a subtractor and carries out subtraction processing of the output of the motion compensation circuit 1305, and the output of the blocking circuit 1301. the difference -- in other than I-picture, a value is inputted into the DCT circuit 1302 through a switch 1310, and coding is performed.

[0053] Moreover, 1307 is a rate control circuit and the amount control of signs is performed from changing the quantization step of a quantizer 1303 based on the occupation of the sign in a buffer 1308. 1315 is an addition circuit, adds the various headers mentioned above to the code data outputted from the buffer 1308, and outputs them to it as MPEG data.

[0054] Drawing 8 is the block diagram showing the example of a configuration of MPEG decode equipment, and 1401 is an input buffer and memorizes the inputted MPEG data temporarily. 1402 is a variable-length decoder (henceforth "VLD"), and decodes the code data read from the input buffer 1401 one by one. 1403 is a reverse quantizer and carries out reverse quantization of the data decoded by VLD1402. 1404 is IDCT, performs Reverse DCT to the data by which reverse quantization was carried out with the reverse quantizer 1403, and changes it into the data of a space field. 1405 -- a motion compensation circuit -- it is -- a switch 1408 -- minding -- data -- inputting -- the difference for motion compensations -- a value is outputted. the difference which 1407 is an adder and was outputted to the output of the reverse DCT circuit 1404 from the motion compensation circuit 1405 -- a value is added. In addition, based on the coding identification code detected by the data detector which is not illustrated, in the case of I-picture, Contact a is chosen, and, in other than I-picture, a switch 1408 chooses Contact b. Therefore, in the case of I-picture, the output of the IDCT circuit 404 is sent to an output buffer 1406, and, in other than I-picture, the output of an adder 1407 is sent to an output buffer 1406.

[0055] Thus, the decoded data are once memorized by the output buffer 1406, and further, it is restored to the original spacial configuration and they are outputted as image data of one frame.

[0056] [An ATM format], next an ATM communication link format are explained.

[0057] Drawing 2 B is drawing showing an ATM communication link format, a series of bit streams are divided into two or more fixed-length packets, and each packet consists of ATM cels of plurality (four [for example,]). An ATM cel consists of a packet header and a pay load for data, generally, a header is made into 5 bytes and data are made into 48 bytes. According to this ATM communication link, with the network bit rate, it is suitable for the transmission system which intermingles for them and transmits various data to independence (asynchronous) since data can be transmitted and a transmission rate can be set as arbitration with the number of transmission cels per unit time amount.

[0058] Although the configuration of a [personal computer], next the personal computer 1115 shown in drawing 1 is explained, the personal computer 1115 is selectively equipped with the Multibus system using the optimal data bus according to the data size of the data transmitted in order to perform various functions, and the transfer rate which processing takes while treating various kinds of data which were mentioned above. In this example, it has the 128-bit data bus D4 and the system bus SB as the data bus D3 of 2 or 64 bits of data buses D of 1 or 32 bits of 16-bit data buses D, and an expansion bus. Moreover, in order to make expansion possible, the personal computer 1115 is equipped with the add-in board interface mentioned later, and can aim at the escape of a device with various kinds of add-in boards connected to this interface.

[0059] 1501 is a network interface (I/F), 1502 is an ATM controller, and various data are delivered [drawing 10 is the block diagram showing the example of a configuration of a personal computer 1115 and] and received through these transmission channels shown in drawing 1, such as the ATM network 1101 and LAN1103, and in between. Moreover, the ATM controller 1502 performs various communications controls, such as a congestion control not only in the function as an ATM switch but the ATM network 1101.

[0060] 1503 is CPU and controls the whole equipment according to the program beforehand stored in

ROM1506. Moreover, CPU1503 is equipped with the bus controller 1504 which constitutes a Multibus system as a factice CPU, and the bit converter 1505. This Multibus system obtains required processing speed by using which data bus properly suitably according to the data size and processing speed to process.

[0061] 1507 is a memory controller, and delivers and receives data between the external storage 1509 which has hard disk drive unit 1508A, CD-ROM drive1508B, etc. 1510 is an edit controller and performs phase management of the data in the time of image edit etc.

[0062] 1511 is a display controller and displays delivery and an image on display devices, such as CRT display 1513 and the FLC display 1514, for image data through memory 1512A. Moreover, a display controller 1512 processes suitably according to the class of display device. 1515 makes delivery and an image print image data on the hybrid printer 1517 equipped with the print section of the method with which it is a printer controller and a thermal transfer printer 1516 differs from an ink jet, hot printing, etc. through memory 1512B. In addition, a printer controller 1515 uses both printers properly according to the image data to print. In addition, memory 1512A and 1512B can be used as one memory, and a display controller 1511 and a printer controller 1515 can also be made to use in common.

[0063] 1518 is CODEC which performs coding/decode of data, and supports a JPEG method and an MPEG method which were explained previously. 1519 is an add-in board interface, and as mentioned above, it can extend the function of a personal computer 1115 by connecting various kinds of add-in boards 1520, 1521, and 1522 here.

[0064] 1523 is an input device controller and connects a keyboard 1524 and a mouse 1525. 1526 is the speech processing section, processes a sound signal and outputs it to a loudspeaker 1527. 1528 is a system port and the tablet 1529, the microphone 1530, the video camera 1531, and scanner 1532 for the hand entry force are connected.

[0065] Since the personal computer 1115 of such a configuration is equipped with the Multibus system which consists of the multi-data buses D1, D2, D3, and D4, a bus controller 1504, and a bit transducer 1505 as mentioned above, based on the transfer and processing speed which is needed according to data size or processing, the optimal data bus can be selectively used for it. Moreover, the processing corresponding to these profiles is also easily attained by connecting the CODEC board which performs coding and the decode corresponding to each profile which could extend the function, for example, was mentioned above with the add-in board by which a personal computer 1115 is connected to the add-in board interface 1519.

[0066] - Explain the configuration of CODEC, next CODEC1518.

[0067] Drawing 11 is the block diagram showing the example of a configuration of CODEC1518, 2600 is a data bus, 2601 is a system bus, and each functional block is connected mutually. Moreover, a system bus 2600 and the system bus SB of personal computer 1115 body are combined through an interface 2602, and a data bus 2600 and each data bus of personal computer 1115 body are combined through the interface 2602. 2616 is a bus arbiter and arbitrates the data bus 2600 in pipeline processing etc.

[0068] 2604 is CPU which performs motion control of the CODEC518 whole, controls each functional block based on the program beforehand memorized by RAM2605, and performs coding and decode processing.

[0069] 2606 is a code detector and detects the control code and code data in input code data, such as a start code (time code) and various headers. After each detected code is memorized by the parameter memory 2607 while it was used through the data bus 2600 or the system bus 2601 as information which is sent to CPU1604 and controls actuation, it is suitably sent to a predetermined block.

[0070] the difference of DC component [2608 is a motion compensation unit, use the reference buffer

2615, and perform the motion compensation of P-picture at the time of coding and decode and B-picture, and also] in JPEG coding -- actuation which calculates a value is also performed.
[0071] The conversion unit with which 2609 is equipped with a rate control unit and 2610 is equipped with a coding buffer, and the DCT machine and reverse DCT machine (IDCT) of plurality [2611 / 2612 / a decode buffer and], the quantization unit with which 2613 is equipped with two or more quantizers and reverse quantizers, and 2614 are variable-length-coding units equipped with two or more VLC(s) and VLD(s). Moreover, 2613A is the quantization table of the quantization unit 2613, 2614A is the Huffman table of the variable-length-coding unit 2614, and in case a unit processes, various parameters, such as a complement child-ized step and a Huffman code, are suitably supplied to these tables from the parameter memory 2607.
[0072] CPU2604 of CODEC1518 equipped with such functional block operates a predetermined unit according to carrier beam directions from CPU1503 of personal computer 1115 body, and performs coding or decode. Specifically, it is the input image data transmitted through the coding buffer 2610, or the motion vector data outputted from the motion compensation unit 2608 and difference -- in the conversion unit 2612, the quantization unit 2613, and the variable-length-coding unit 2614, after a value (code data-ed) is stored in the decode buffer 2611 which is processed and functions as an output buffer one by one, it is the predetermined timing directed from CPU2604, and is outputted from CODEC1518 through a data bus 2600 and an interface 2603.
[0073] On the other hand, in the variable-length-coding unit 2614, the quantization unit 2613, and the conversion unit 2612, one by one, after the code data (decoded data) transmitted through the decode buffer 2611 is stored in the coding buffer 2610 which is processed and functions as an output buffer, it is the predetermined timing directed from CPU2604, and is outputted from CODEC1518 through a data bus 2600 and an interface 2603.
[0074] CODEC1518 performs data transfer control to each unit, and motion control of each unit using the optimal sequence according to various kinds of processing modes, the case where two or more coding or decode is performed simultaneously, when carrying out parallel processing of the decode to coding, or when it is parallel and performs various processings, such as a communication link, a display, and print-out, and coding and the decode in personal computer 1115 body. In addition, the program of operation corresponding to these sequences is beforehand memorized by RAM2605 which consists of a static RAM or RAM by which the battery back-up was carried out. Moreover, the program memorized by RAM2605 can be updated if needed.
[0075] [The configuration of a color copying machine], next the configuration of the image processing system of color copying machines 1109 and 1119 are explained.
[0076] - Reader section drawing 12 A and drawing 12 B are the block diagrams showing the example of a configuration of an image processing system.
[0077] In this drawing, 201 is a CCD sensor, is the three-line CCD sensor equipped with the filter of RGB 3 color, and reads a manuscript image. 202 is the sample hold & A/D-conversion section, and changes each into a 8-bit digital RGB picture signal the analog RGB picture signal inputted from the CCD sensor 201. 203 is the shading compensation section and performs a shading compensation to the picture signal by which A/D conversion was carried out. 204 is the bond amendment &MTF amendment section, and performs phasing of the direction of vertical scanning of RGB each color of the CCD sensor 201, optical amendment of distortion, and gap amendment of the direction of vertical scanning at the time of variable power to the picture signal by which the shading compensation was carried out. 206 is the input masking section and changes into the RGB picture signal suitable for equipment the RGB picture signal with which amendment mentioned above was performed.
[0078] 232 is a bus selector and chooses the picture signal outputted from the input masking section 206, or the picture signal inputted through external I/F231 with the selection signal from the control section of the image processing system which is not illustrated. In addition, external I/F231 is general

interfaces, such as a network interface for connecting with the ATM network 1101 or LAN1103 or Centronics, SCSI and GPIB, RS232C, and RS422. Moreover, the bus selector 232 can also send the picture signal inputted from the input masking circuit 206 to external I/F231, and a host machine (for example, personal computer 1115) etc. can also obtain the image data which read the manuscript through external I/F231.

[0079] 207 is a color space compression zone, and it removes a substrate (lower color) while it compresses the color reproduction range of the picture signal inputted from the bus selector 232 according to the color reproduction range of the device which outputs an image. 208 is the variable power section and performs mirror image processing changed into the variable power processing and the mirror image which expand an image to the picture signal with which the color reproduction range was compressed if needed. 210 is a compression zone, encodes the picture signal inputted from the variable power section 208, and stores it in the memory section 211. The encoded picture signal which was stored in the memory section 211 is read by the four image formation sections 233m, 233c, 233y, and 233k synchronizing with the output of the printer section mentioned later, and a MCYK picture signal is formed. In addition, since the four image formation sections 233m, 233c, 233y, and 233k are equipped with the same configuration, below, they explain 233m of M image formation sections, and omit other explanation.

[0080] 212 is the expanding section and decodes the encoded picture signal which was inputted from the memory section 211. In addition, when lossy compression of the original picture signal is carried out, image quality may deteriorate by this expanding. 222 is a bus selector and chooses the picture signal outputted from the expanding section 212, or the picture signal outputted from the variable power section 208 with the selection signal from the control section of the image processing system which is not illustrated. 219 is a LOG converter and changes into a 8-bit MCY picture signal the RGB picture signal inputted from the bus selector 222. 213 is masking and the UCR section, performs output masking processing and UCR processing to the picture signal inputted from the LOG converter 219, for example, outputs 8-bit M picture signal.

[0081] 214 is the variable power section and performs variable power processing which reduces an image to M picture signal inputted from masking and the UCR section 213 if needed. 215 is the gamma correction section and performs a gamma correction to M picture signal inputted from the variable power section 214 according to the color reproduction property of the device which outputs an image. 216 is the smoothing section and performs smoothing processing for the object of removing moire to M picture signal to which the gamma correction was performed. 217 is the edge enhancement section and emphasizes edges contained in M picture signal with which smoothing processing was performed, such as an alphabetic character and a line drawing.

[0082] 220 is incompressible memory and memorizes the picture signal inputted from the edge enhancement section 217. 221 is a selector and chooses the picture signal outputted from the edge enhancement section 217, or the picture signal outputted from incompressible memory with the selection signal from the control section of the image processing system which is not illustrated. 218 is the video-processing section and changes M picture signal inputted from the selector 221 into the signal according to the device which outputs an image. For example, when image output equipment is a laser beam printer, in order to drive a laser component, the drive signal which performed pulse width modulation according to the inputted picture signal is outputted.

[0083] - The block diagram 13 of the printer section is general-view drawing of the color copying machines 1109 and 1119 shown in drawing 1, and is roughly divided into two configurations. 101 is the reader section, and as mentioned above, it is a part which reads a color copy image and performs an image processing further. 103 is the printer section, is equipped with different image support and reproduces a color picture according to the digital image signal of each color sent from the reader section 101. In addition, the manuscript feeder 102 set to the reader section 101 is a well-known

option device which conveys a manuscript automatically to the manuscript reading area of the reader section 101.

[0084] 301 is a polygon scanner, detects the laser beam scanned by the beam detection sensor (it is called "BD sensor" un-illustrating and the following), and generates a horizontal-scanning synchronizing signal while it scans the laser beam which emitted light with four laser components (un-illustrating) driven to MCYK independence by the video-processing section 218 on the photoconductor drum of the image formation section corresponding to each color. As for M image formation section and 303, C image formation section and 304 form [302] the image of a color with which Y image formation section and 305 are K image formation sections, and correspond, respectively. Since the configuration of the image formation sections 302-305 is abbreviation identitas, the detail of M image formation section 302 is explained below, and explanation of other image formation sections is omitted.

[0085] In M image formation section 302, 318 is a photoconductor drum and a latent image is formed in the front face of the laser beam from the polygon scanner 301. 315 is a primary electrification machine, electrifies the front face of a photoconductor drum 318 in predetermined potential, and prepares latent-image formation. 313 is a development counter, develops the latent image on a photoconductor drum 318, and forms a toner image. In addition, the sleeve 314 for developing negatives by impressing development bias is contained in the development counter 313. 319 is an imprint electrification machine, performs discharge from the tooth back of the imprint belt 306, and imprints the toner image on a photoconductor drum 318 to the recording paper on the imprint belt 306 etc. The photoconductor drum 318 after an imprint has the front face cleaned by the cleaner 317, and is discharged with the auxiliary electrification vessel 316, and good electrification comes to be further acquired with the primary electrification vessel 315 again by eliminating residual charge with the pre-exposure lamp 330.

[0086] Next, the procedure which forms an image in up to the recording paper etc. is explained. 308 is the feed section and supplies the detail paper stored in the cassette 309,310 to the imprint belt 306. The recording paper supplied from the feed section 308 is electrified by the adsorption zone electrical machinery 311. 312 is an imprint belt roller, drives the imprint belt 306, and becomes the adsorption zone electrical machinery 311 and a pair, electrifies the detail paper etc., and makes the detail paper etc. stick to the imprint belt 306. 329 is a paper head sensor and detects heads, such as the recording paper on the imprint belt 306. In addition, the detecting signal of the paper head sensor 329 is used as a vertical-scanning synchronizing signal by that at the time of being sent to the reader section 101 from the printer section 103, and sending a video signal to the printer section 103 from the reader section 101.

[0087] Then, the detail paper etc. is conveyed with the imprint belt 306, and a toner image is formed in that front face in order of MCYK in the image formation sections 302-305. After electricity is discharged with the electric discharge electrification vessel 324, the detail paper which passed K image formation section 305 is separated from the imprint belt 306, in order to make separation from the imprint belt 306 easy. 325 is an exfoliation electrification machine and prevents the image turbulence by the exfoliation discharge at the time of the detail paper etc. dissociating from the imprint belt 306. The separated recording paper is discharged, after being charged with the electrification vessel 326,327 before fixation and heat fixation of the toner image is carried out by the fixing assembly 307, in order to compensate the adsorption power of a toner and to prevent image turbulence. 340 is a delivery sensor and it detects that the recording paper etc. was discharged.

[0088] - The compression method in the data compression section of data compression section this example differs from the compression method standardized [JPEG]. That is, since the frequency of occurrence of image data, such as an alphabetic character and a thin line, is comparatively high in the image which an image processing system treats, a method with which these image data is reproduced

more by validity has been adopted. Furthermore, the picture compression method suitable for an image processing system which enabled it to be managed even if it made it fixed length coding and did not carry out adjustable [of the output speed of image data] is adopted.
[0089] Drawing 14 is drawing for explaining coding which a compression zone 210 performs, that one measure is equivalent to 1 pixel, and this 1 pixel consists of 8 bits of RGB each. 4x4 pixels these a total of 16 pixels are made into 1 block, and 16 pixel x3 color x8 bit =384 bit data are compressed into one sixth, and it is made 64-bit fixed length data. The vector quantization and orthogonal transformation coding which are mentioned later are used for this coding.
[0090] - Color space conversion section drawing 15 is the block diagram showing the detailed example of a configuration of a compression zone 210 and 212m of expanding sections.
[0091] In this drawing, 401 is a color space conversion machine and changes into the lightness signal L and chromaticity signals a and b the RGB picture signal inputted into the compression zone 210. A Lab signal is a signal showing the uniform color space specified in CIE, and is expressed with a degree type here.

$$\begin{bmatrix} L \\ a \\ b \end{bmatrix} = \begin{bmatrix} 0 & \alpha 12 & 0 \\ \alpha 21 & \alpha 22 & 0 \\ 0 & \alpha 32 & \alpha 33 \end{bmatrix} \begin{bmatrix} (X/X0)^{(1/3)} \\ (Y/Y0)^{(1/3)} \\ (Z/Z0)^{(1/3)} \end{bmatrix} + \begin{bmatrix} \alpha 14 \\ 0 \\ 0 \end{bmatrix} \quad \cdots(1)$$

However, in alphaij, and X0, Y0 and Z0, constant a^b expresses the b-th power of a. [0092] X, Y, and Z of a top type are the signal which calculates an RGB code and is generated, and are expressed by the degree type.

$$\begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = \begin{bmatrix} \beta 11 & \beta 12 & \beta 13 \\ \beta 21 & \beta 22 & \beta 23 \\ \beta 31 & \beta 32 & \beta 33 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix} \quad \cdots(2)$$

However, betaij is a constant. [0093] 402 is a lightness signal encoder, encodes the lightness signal L per 4x4 pixel block, and outputs code-signal L-code and attribute signal E-code which shows whether this pixel block is the edge section. 403 is a chromaticity signal letter-ized machine, encodes chromaticity signals a and b per 4x4 pixel block, and outputs code-signal ab-code.
[0094] These code signals are stored in the memory section 211, and are read by the expanding section 212. 404 is a lightness signal decoder and decodes the lightness signal L from inputted code-signal L-code. 405 is a chromaticity signal decoder and decodes chromaticity signals a and b from inputted code-signal ab-code. 406 is a color space conversion machine and changes the decoded Lab picture signal into the original RGB picture signal. It changes into each color component of M, C, Y, and K which are a toner development color. 407 is a logarithmic transformation machine and changes into a MCY picture signal the RGB code inputted from the color space conversion machine 406.
[0095] - The block diagram in which lightness signal encoder drawing 16 shows the detailed configuration of the lightness signal encoder 402, drawing 17, and 18 are drawings showing the concept of lightness signal coding.
[0096] Coding (compression) of image data performs a total of the 16-pixel block of 4 pixel x vertical scanning of four lines of horizontal scanning as a unit, as shown in drawing 14. Here, XPHS repeats 0, 1, 2, and 3 by the 2-bit signal which shows a horizontal-scanning location, and YPHS repeats 0, 1,

2, and 3 by the 2-bit signal which shows a vertical-scanning location, and as shown in drawing, the pixel block of 4x4 is started synchronizing with Signals XPHS and YPHS.

[0097] First, the concept of lightness signal coding is explained using drawing 17 and 18. If the Hadamard transform of 4x4 shown in (3) types is performed to the lightness information Xij (i, j= 1, 2, 3, 4) started by 4x 4-pixel block shown in drawing 17 (a), Yij (i, j= 1, 2, 3, 4) shown in drawing 17 (b) will be obtained. A Hadamard transform is a kind of orthogonal transformation, develops the data of 4x4 by the 2-dimensional Walsh function, and is equivalent to the signal of a time domain or a space field being changed into a frequency domain or a spatial-frequency field by the Fourier transform. That is, the matrix Yij (i, j= 1, 2, 3, 4) after a Hadamard transform becomes a signal equivalent to each component of the spatial frequency which the matrix Xij (i, j= 1, 2, 3, 4) of an input signal has.

$$\begin{bmatrix} Y11 & Y12 & Y13 & Y14 \\ Y21 & Y22 & Y23 & Y24 \\ Y31 & Y32 & Y33 & Y34 \\ Y41 & Y42 & Y43 & Y44 \end{bmatrix} = (1/4)\cdot H^{T}\cdot \begin{bmatrix} X11 & X12 & X13 & X14 \\ X21 & X22 & X23 & X24 \\ X31 & X32 & X33 & X34 \\ X41 & X42 & X43 & X44 \end{bmatrix} \cdot H \quad \cdots(3)$$

However, for H, Hadamard-matrix H^T of 4x4 is the transposed matrix of H.

$$H = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \\ 1 & -1 & 1 & -1 \end{bmatrix}$$

[0098] Here, like the case of the 2-dimensional Fourier transform, the more the value (namely, line number) of i becomes large, a spatial-frequency component high in the direction of vertical scanning is arranged, and the more the value (namely, aisle location) of j becomes large, the more as for the Hadamard transform result Yij (i, j= 1, 2, 3, 4), a spatial-frequency component high to a main scanning direction is arranged. Especially in the case of i=j=1, it is set to Yij=(1/4) sigmaXij, and the signal (signal of the value which doubled the average four strictly) equivalent to the dc component, i.e., the average, of input data Xij (i, j= 1, 2, 3, 4) is outputted.

[0099] As for the image generally read with the image scanner, it is known with the resolution of reading sensors, such as CCD, the transparency property of optical system, etc. that there are few high spatial-frequency components. Using the sensibility of a spatial-frequency component also with the still higher visibility property of human being's eyes being low, the signal Yij (i, j= 1, 2, 3, 4) after a Hadamard transform is formed into a scalar quantity child, and Zij (i, j= 1, 2, 3, 4) shown in drawing 17 (c) is obtained.

[0100] Drawing 18 (a) the number of bits of each element of the lightness information Xij (i, j= 1, 2, 3, 4) Although this drawing (b) shows the number of bits of each element of the AMADARU conversion result Yij (i, j= 1, 2, 3, 4) and this drawing (c) shows the number of bits of each element of Zij (i, j= 1, 2, 3, 4) as a result of scalar quantity child-ized As shown in this, Y11, i.e., a dc component, is quantized with the most numbers of bits (8 bits). It is referred to as Z11 and a component with higher spatial frequency is quantized with the small number of bits. Furthermore, as shown in drawing 17 (d), grouping of the 16 elements of zij (i, j= 1, 2, 3, 4) is carried out to a dc component and four alternating current components. That is, as shown in a table 1, a dc component Z11 is assigned to Signal AVE, The high-frequency components Z24, Z34, Z42, Z43, and Z44 of horizontal scanning

which carried out grouping of the mid-range alternating current components Z22, Z23, Z32, and Z33 of horizontal scanning which carried out grouping of the vertical-scanning alternating current components Z21, Z31, and Z41 which carried out grouping of the horizontal-scanning alternating current components Z12, Z13, and Z14 which carried out grouping to the signal L1 to allocation and a signal L2 to allocation and Signal M, and vertical scanning to allocation and Signal H, and vertical scanning are assigned.

[0101]

[A table 1]

信号名	成分	要素
AVE	直流成分(平均值)	Z11
L1	主走查交流成分	Z12 Z13 Z14
L2	副走查交流成分	Z21 Z31 Z41
M	主副中域交流成分	Z22 Z23 Z32 Z33
H	主副高域交流成分	Z24 Z34 Z42 Z43 Z44

Furthermore, code length is changed by whether it is that the pixel block concerned is the edge section in an image, and it encodes for every group. For example, in the case of the edge section, it is the code length who shows an example to drawing 18 (d), and, in the case of the non-edge section, encodes by the code length who shows an example in this drawing (e), respectively. That is, in the edge section, since the information on an alternating current component is important, many code length is assigned to the alternating current component signals L1, L2, M, and H.

[0102] In drawing 16, 701,702,703 is line memory, respectively and a pixel block as shown in drawing 14 is started by delaying the image data of one line at a time. 704 is a Hadamard transform circuit and performs conversion shown in (3) types. That is, synchronizing with Signal CLK and XPHS, the data with which the data with which the data with which X11 and the data equivalent to X12, X13, and X14 are equivalent to terminal x2 X21, X22, X23, and X24 are equivalent to a terminal x3 X31, X32, X33, and X34 are equivalent to a terminal x4 X41, X42, X43, and X44 are inputted into the terminal x1 of the Hadamard transform circuit 704, respectively. The signal by which the Hadamard transform was carried out is delayed by eight pulses of Signal CLK, Y21, Y22, Y23, and Y24 are outputted for Y11, Y12, Y13, and Y14 from a terminal y2 from a terminal y1, and Y41, Y42, Y43, and Y44 are outputted for Y31, Y32, Y33, and Y34 from a terminal y4 from a terminal y3, respectively.

[0103] 705 to 708 is LUT, respectively, for example, consists of ROMs etc., and performs scalar quantity child-ization mentioned above. That is, according to the Hadamard transform result and Signal XPHS which were inputted into address terminal A, in order to quantize to the number of bits as shows the output by which the Hadamard transform was carried out to 708 to drawing 18 (c) from LUT705, data are beforehand written in so that a scalar quantity child-ized result may be outputted.

[0104] 709 is a grouping circuit and performs grouping for vector quantization. Drawing 19 is the block diagram showing the detailed example of a configuration of the grouping circuit 709.

[0105] In this drawing, 101 to 116 is a flip-flop (henceforth "F/F"), respectively, and holds each 4x4-block data which shows the inputted signal to drawing 17 (c) by being delayed synchronizing with Signal CLK. And it divides into the group who shows the held data in a table 1, and each data of Signals AVE, L1, L2, M, and H is extracted.

[0106] It is the selector of 2 input 1 output, 117 to 121 outputs the signal inputted into Terminal A, respectively, when '0' is inputted into the selection terminal S, and when '1' is inputted, it outputs the

signal inputted into Terminal B. The signal XD0 inputted into the selection terminal S is set to '0' only within the case where Signal XPHS is '0', synchronizing with Signal CLK and XPHS, and is a signal set to '1' except it. Therefore, the scalar quantity child-ized result for every group shown in a table 1 is outputted from selectors 117-121 every 4x4 blocks.

[0107] what quantizes the signals L1, L2, M, and H which 710 to 713 is LUT, for example, consisted of ROMs etc. in drawing 16 again, and were outputted from the grouping circuit 709, respectively by well-known vector quantization -- it is -- a group L1 -- 9 bits -- a group L2 -- 9 bits -- Group M -- 8 bits -- Group H -- 8 bits -- respectively -- quantizing -- in all [of AVE / 8 bits and] -- it is made a total of 43 bits.

[0108] Although mentioned later for details, the signal ED 1 inputted into address terminal A of each LUT here is a signal which shows whether the pixel block concerned is the edge section. the case where a signal ED 1 is inputted into the upper address of each LUT, Signals L1, L2, M, and H are inputted into a lower address, respectively, and the pixel block concerned is the edge section -- a group L1 -- 9 bits -- a group L2 -- 9 bits -- Group M -- 9 bits -- Group H -- 8 bits -- respectively -- quantizing -- in all [of AVE / 8 bits and] -- it is made a total of 43 bits. moreover, the case where the pixel block concerned is the non-edge section -- a group L1 -- 8 bits -- a group L2 -- 8 bits -- Group M -- 8 bits -- Group H -- 7 bits -- respectively -- quantizing -- in all [of AVE / 8 bits and] -- it is made a total of 39 bits.

[0109] furthermore, a quantization result is inputted into F/F714, is held in the start of a signal CLK4 (XPHS= -- the time of 0 and 1 -- '1' -- XPHS= -- set to '0' at the time of 2 and 3), and is outputted as L-code to predetermined timing.

[0110] On the other hand, 715 is a LGAIN calculation machine and is the same timing as the Hadamard transform circuit 704, Per 4x4 blocks, the lightness information Xij (i, j= 1, 2, 3, 4) is inputted into the terminals A, B, C, and D, and LGAIN showing the amplitude (maximum-minimum value) of the lightness signal L, LMX showing the location (coordinate within a pixel block) where the lightness signal L becomes maximum, and LMN showing the location (coordinate within a pixel block) where the lightness signal L becomes the minimum value are computed, respectively.

[0111] 716 is a comparator, compares the threshold Th beforehand set to Signal LGAIN and the fixed value register 717, and outputs the comparison result ED. That is, when a pixel block is the edge section, Signal ED is set to '1' by LGAIN>Th, and when a pixel block is the non-edge section, Signal ED is set to '0' by LGAIN<Th. 718-720 are F/F, respectively and acquire the signal ED 1 which it is [signal] delayed synchronizing with the start of a signal CLK4, and synchronized the inputted signal ED with the timing of the above-mentioned vector quantization. 721 is delayed by F/F in the inputted signal ED 1 synchronizing with the start of a signal CLK4, and a signal E-code signal is outputted.

[0112] - Chromaticity signal letter-ized machine drawing 20 is the block diagram showing the detailed example of a configuration of the chromaticity signal letter-ized machine 403.

[0113] In this drawing, 729 to 731 is line memory, respectively, gives delay for one line to the inputted chromaticity signal a, and makes this signal a 4x4-pixel block. 724 is a quantizer and quantizes a of the 4x4-pixel block inputted from the line memory 729,730,731.

[0114] Similarly, 725 to 727 is line memory, respectively, gives delay for one line to the inputted chromaticity signal b, and makes this signal a 4x4-pixel block. 728 is a quantizer and quantizes b of the 4x4-pixel block inputted from the line memory 725-727.

[0115] The output amean, i.e., the signal, Signal again and Signal bmean, and Signal bgain of quantizers 724 and 728 are unified, and become ab-code. Here, Signal amean is the dc component of a, Signal again is the alternating current component of a, Signal bmean is the dc component of b and Signal bgain is the alternating current component of b. In addition, the delay circuit which is not illustrated for taking the lightness information encoder 402 and a synchronization is established in the latter part of the chromaticity information encoder 403, and signal L-code and ab-code are in phase,

and are outputted from a compression zone 210.

[0116] Drawing 21 and 22 are the block diagrams showing the detailed example of a configuration of a quantizer 724 or a quantizer 728.

[0117] In this drawing, 601 to 624 is F/F, is delayed by six pulses in each of four input signals synchronizing with the start of Signal CLK, respectively, and performs synchronous doubling with the lightness information encoder 402.

[0118] 625 and 626 are the signal which was the selector of 4 input 1 output, and was inputted into Terminal A when "0" was inputted into Terminal S. The signal inputted into Terminal D when the signal inputted into Terminal C when the signal inputted into Terminal B when "1" was inputted was inputted into "2" was inputted into "3" is chosen, respectively, and is outputted. 2 bits (that is, bits 3 and 2) of high orders of Signal LMX are inputted into the terminal S input of a selector 625, and 2 bits (that is, bits 3 and 2) of high orders of Signal LMN are inputted into the terminal S of a selector 616.

[0119] On the other hand, 630 is F/F, respectively and is delayed from 627 by four pulses synchronizing with the start of Signal CLK in inputted 2 bits (that is, bits 1 and 0) of low order of Signal LMN and 2 bits (that is, bits 1 and 0) of low order of Signal LMX. 634 is delayed from 631 by F/F by 1 to 4 pulses in the signal inputted from the selector 625 synchronizing with the start of Signal CLK, respectively. 638 is delayed from 635 by F/F by 1 to 4 pulses in the signal inputted from the selector 626 synchronizing with the start of Signal CLK, respectively.

[0120] 639 and 640 are the selectors of 4 input 1 output, and a selector 639 is, It responds to 2 bits of low order of the signal LMX which was inputted into the selection terminal S from F/F630 and which synchronized. Choosing and outputting the signal inputted from either of 634 from F/F631, a selector 640 chooses and outputs the signal inputted from either of 638 from F/F635 according to 2 bits of low order of the signal LMN which was inputted into the selection terminal S from F/F630 and which synchronized. The value of the chromaticity signals a or b of a location (coordinate) with which the lightness signal L becomes maximum within a 4x4-pixel block is outputted as a signal MX from a selector 639 as a result, and the value of a or b of the location (coordinate) where the lightness signal L becomes the minimum value is outputted as a signal MN from a selector 640.

[0121] On the other hand, 641 is an averaging machine and outputs the average (A+B+C+D)/4 of the signal inputted into D from the input terminal A. 642 to 645 is F/F and is delayed from 1 by four pulses in the signal inputted from the averaging machine 641 synchronizing with the start of Signal CLK. 646 is an averaging machine and outputs the average (A+B+C+D)/4 of the signal inputted into D from the input terminal A from each of F/F622 to 645 as a signal ME. As a result, the average of a or b within a 4x4-pixel block is outputted as a signal ME.

[0122] On the other hand, 647-650 are F/F, are delayed by four pulses synchronizing with the start of Signal CLK, and output the inputted signal LGAIN as a signal LG synchronizing with each signals MX, MN, and ME. In drawing 11, each signals MX, MN, ME, and LG synchronize in the start of Signal CLK in 654 from F/F651.

[0123] 655 is a subtractor and subtracts Signal MN from Signal MX. that is, the difference of the signals a or b in the location where Signal L becomes maximum within a 4x4-pixel block, and the location which becomes the minimum value -- MX-MN is outputted. 657 is LUT and is outputted to the upper address terminal from F/F656 -- having -- the difference of Signals a or b -- MX-MN is inputted, it is outputted to the lower address terminal from F/F661, and Signal LG is inputted. The data which quantized the ratio (MX-MN) of amplitude MX-MN of the alternating current component of the chromaticity signals a or b within a 4x4-pixel block and the amplitude LG of the alternating current component of the lightness signal L / value of LG to the triplet are written in beforehand, and LUT657 outputs these data according to an input.

[0124] The selector of 2 input 1 output, 659, and 663-667 are F/F, and 658 and 662 output Signal gain and Signal mean to predetermined timing as a result.

[0125] - It is drawing showing an example of the code length of the 4x4-pixel block in the coding method of the image processing system which shows drawing 23 to drawing 12 A and drawing 12 B about code length. In addition, although the outline was explained above, code length's allocation can also be changed according to whether the pixel block concerned is the edge section, and this drawing shows an example to which code length's allocation is changed. Specifically, code length when 12 is judged as the pixel block concerned being the non-edge section in code length when 11 is judged as the pixel block concerned being the edge section is shown, respectively.
[0126] 1 bit is assigned to E-code which is the judgment signal of whether the top pixel block concerned is the edge section. Moreover, 8 bits is assigned to the signal AVE which is the dc component of the lightness information L.
[0127] In the edge section, since the alternating current component information on the lightness information L becomes important, and 9, 9, and 9 or 8 bits are assigned than the non-edge section, respectively. [number of bits / which is assigned to the signals L1, L2, M, and H which show an alternating current component] In addition, in the non-edge section, they are 8, 8, and 8 or 7 bits, respectively.
[0128] On the other hand, it assigns 8 bits each to the signals amean and bmean which show the dc component of the chromaticity information a and b in 6 bits each and the non-edge section by the edge section. This is because the information on the dc component in the non-edge section is more important than it in the edge section. Moreover, the edge section and the non-edge section assign 4 bits to the signals again and bgain which show the alternating current component of chromaticity information respectively.
[0129] Since a total of 39 bits is assigned to the lightness information L to the lightness information L at a total of 43 bits and the chromaticity information a and b and it assigns a total of 24 bits to the chromaticity information a and b as a result when the pixel block concerned is the edge section, and allocation and the pixel block concerned are the non-edge sections about a total of 20 bits, together with judgment signal E-code of whether to be the edge section, it becomes a total of 64-bit fixed length's sign.
[0130] - Equipment timing-chart drawing 24 is the example of an equipment timing chart of color copying machines 1109 and 1119.
[0131] In this drawing, Signal START is a signal which shows manuscript reading actuation initiation. The section when an image scanner reads a manuscript image at and Signal WPE performs coding processing and memory write is expressed. Signal ITOP is a signal which shows initiation of printing actuation, and Signals MPE, CPE, YPE, and KPE are section signals which drive Magenta semiconductor laser, cyanogen semiconductor laser, yellow semiconductor laser, and black semiconductor laser, respectively.
[0132] To be shown in this drawing, as for Signals CPE, YPE, and KPE, only time amount t1, t2, and t3 is delayed to Signal MPE, respectively, and this will be controlled by the relation of a degree type, if distance of the medial axis of the photoconductor drum of M image formation section 302 and the medial axis of the photoconductor drum of other image formation sections is set to d1, d2, and d3. t1=d1/v, t2=d2/v, t3=d3/v -- (4), however v are the bearer rate of the recording paper. [0133] Signal HSYNC is a horizontal-scanning synchronizing signal, and Signal CLK is a pixel synchronizing signal. Signal YPHS is the counted value of a 2-bit horizontal-scanning counter. Signal BLK is a synchronizing signal of a 4x4 pixel block unit, and processing is made per 4x4 blocks to the timing shown by BDATA.
[0134] - Memory section drawing 25 is the block diagram showing the example of a configuration of the memory section 211.
[0135] 180 is a memory address controller and consists of memory control sections 186 which generate the selector 184 which changes the output of the updown counter 182 of a main scanning

direction (the direction of X), the updown counter 183 of the direction of vertical scanning (the direction of Y), and both counters, the coordinate-address translation machine 185 which changes the counted value into the address of memory 187 (for example, it consists of DRAMs) and a signal/RAS, /CAS, and /WA (any -- a low -- active).

[0136] Here, if the select signal of a selector 184 is set to ROT0 and rise/down change-over signal of two updown counters is set to ROT1 and ROT2, respectively, eight kinds of images which performed revolution and mirror image processing in which an example was shown in drawing 26, by total of a these 3 bits signal can be outputted from memory 187.

[0137] Furthermore, memory 187 consists of one or more DRAM modules. For example, the case where a DRAM module with data width of face of 16 bits is constituted from four (it becomes a total of 64 bits as well as the code length who mentioned above) is considered.

[0138] Data width of face is the same, and prepares two or more kinds (for example, the object for compression and for incompressible) for the DRAM module with which address spaces differ. For example, when it is going to store the image of A3 size by 400dpi (pixel spacing of about 63.5 micrometers), and 8 bits of each RGB, the memory size of about 96 M bytes (that is, 8 bit x3 of address 32 M bit x data color) is needed. As mentioned above, when it compresses into one sixth per 4 pixel x four lines to it, it ends with the memory size of about 16 M bytes (64 bits of that is, address 2 M bit x data). Therefore, in order to store the image information of the same A3 size, what is necessary will be just to use the DRAM module of a 21-bit address space by the data compression system using the DRAM module with which a 25-bit address space is by the data incompressible system.

[0139] However, when it is incompressible 400 dpi and carries out addressing of the image information of A3 size, since it is 297mm (= 4,677 pixels) and the direction of vertical scanning (Y) is 420mm (= 6,614 pixels), if a main scanning direction (X) carries out addressing of this simply, it will become a total of 26 bits at the 13 bits of the directions of X, and the 13 bits of the directions of Y. Similarly, when carrying out addressing of the image information of A3 size by 100dpi compression (4 pixel x4 line is made into 1 block), the 11 bits of the directions of X and the 11 bits of the directions of Y make a total of 22 bits, and it does not fit in a 2M bit address space at the time of 32M bit and compression at the above-mentioned time of incompressible.

[0140] Then, the address given to a DRAM module is carried out like drawing 27. namely, the most significant bit (MSB) of the direction of X -- a case -- dividing -- carrying out -- the direction of X -- when MSB is '0', the address of the direction of Y is arranged on the high order of the address except MSB of the direction of X, and what reversed the address of the direction of X on the high order of the address of the direction of Y is arranged at the time of '1'. If it does in this way, the field A part which the space of A3 size is changed into the address space suitable for a DRAM module, namely, is shown in drawing 28 is mapped as it is, and since a field C part is permuted by Field B and mapped, it can utilize an address space effectively without futility. In addition, the coordinate-address translation machine 185 shown in drawing 25 performs this address translation. Furthermore, if the regulation of this conversion method is followed, even if it is 400dpi and is 100dpi, an address space can be used without futility.

[0141] - Lightness signal decoder drawing 29 is the block diagram showing the detailed example of a configuration of the lightness signal decoder 404.

[0142] The lightness signal decoder 404 decodes the lightness information L by decoding and carrying out the reverse Hadamard transform of signal L-code read from the memory section 211. A reverse Hadamard transform is inverse transformation of the Hadamard transform shown by (3) formulas, and is defined by (5) types.

$$\begin{bmatrix} X11 & X12 & X13 & X14 \\ X21 & X22 & X23 & X24 \\ X31 & X32 & X33 & X34 \\ X41 & X42 & X43 & X44 \end{bmatrix} = (1/4)\cdot H^{T}\cdot \begin{bmatrix} Y11 & Y12 & Y13 & Y14 \\ Y21 & Y22 & Y23 & Y24 \\ Y31 & Y32 & Y33 & Y34 \\ Y41 & Y42 & Y43 & Y44 \end{bmatrix} \cdot H \quad \cdots(5)$$

However, for H, Hadamard-matrix H^T of 4x4 is the transposed matrix of H.

$$H = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \\ 1 & -1 & 1 & -1 \end{bmatrix}$$

[0143] On the other hand, a Hadamard transform and a reverse Hadamard transform are linearity operations, and when expressing the Hadamard transform or reverse Hadamard transform of Matrix X as H (X), generally (6) types are realized.
H(X1+X2+ -- +Xn) = H(X1)+H(X2)+ -- +H (Xn) -- (6) [0144] Using this property, it decomposes into each frequency band which the encoder a1113 defined, and a reverse Hadamard transform is performed to juxtaposition, respectively. Here, (7) types will be realized if the data matrix decoded from YM and Sign H in the data matrix decoded from YL2 and Sign M in the data matrix decoded from YL1 and a sign L2 in the data matrix decoded from the sign L1 is set to YH.
H(YL1+YL2+YM+YH) = H(YL1)+H(YL2)+H (YM) +H (YH) -- (7) [0145] In drawing 29, 1601 to 1604 is LUT, respectively, for example, it consists of ROMs etc., and each LUT holds beforehand the result of having computed decode processing and reverse Hadamard transform processing beforehand. the lower address of LUT1601 -- the sign of L1 -- the sign of M is inputted into the lower address of LUT1603, the sign of H is inputted into the lower address of LUT1604 for the sign of L2 in the lower address of LUT1602, respectively, and, on the other hand, Signals XPHS and YPHS and the revolution signal ROT (refer to drawing 26) are inputted into the upper address (7 bits) of each LUT.
[0146] Furthermore, 1605 is an adder, is a part which performs addition equivalent to (7) types, and adds the reverse Hadamard transform result of each frequency component (L1, L2, M, H). An addition result is the alternating current component of the lightness information L within a 4x4-pixel block, and is outputted as an alternating current component signal LAC of the lightness information L through F/F1606.
[0147] When decoding collectively, without using this method, it is not realistic for it realizing by LUT with a bits [a total of 41 bits of a total / of a 34-bit sign /, a 4-bit coordinate (XPHS, YPHS), and the signal ROT of a triplet], i.e., 41 bits, address space (that is, 2T byte) being needed, either. By using the above-mentioned method, a configuration becomes very easy that what is necessary is just to prepare some at most 16 bits (4 bit +ROT signal triplet of 9 bit + coordinates of signs) address space (64 K bytes) ROMs. Moreover, a response is easy also when changing code length.
[0148] 1607 is an adder, is adding the signal LAC inputted from F/F1606, and the average AVE inputted from F/F1609, and acquires the lightness signal L. By F/F1608, the lightness signal L outputted from the adder 1607 synchronizes, and is outputted to the start of Signal CLK.
[0149] - Chromaticity signal decoder drawing 30 is the block diagram showing the detailed example of a configuration of the chromaticity signal decoder 405.
[0150] After signal ab-code read from the memory section 211 synchronizes with the start of Signal

CLK by F/F1701, it is decomposed into a-code and b-code, and it is further decomposed into again, amean, bgain, and bmean.

[0151] The signal again (the ratio of the amplitude of Signal a and the amplitude of Signal L is expressed that it mentioned above) decomposed with the multiplier 1702 is multiplied by the alternating current component LAC of Signal L, the signal amean which is the dc component of Signal a is added with an adder 1704, and Signal a is decoded. By F/F1706, the decoded signal a synchronizes and is outputted to the start of Signal CLK.

[0152] Similarly the signal bgain (the ratio of the amplitude of Signal b and the amplitude of Signal L is expressed that it mentioned above) decomposed with the multiplier 1703 is multiplied by the alternating current component LAC of Signal L, the signal bmean which is the dc component of Signal b is added with an adder 1705, and signal b* is decoded. By F/F1707, decoded signal b* synchronizes and is outputted to the start of Signal CLK.

[0153] - The color space conversion machine color space conversion machine 406 changes a Lab signal into an RGB code by the degree type.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} \beta 11' & \beta 12' & \beta 13' \\ \beta 21' & \beta 22' & \beta 23' \\ \beta 31' & \beta 32' & \beta 33' \end{bmatrix} \begin{bmatrix} X \\ Y \\ Z \end{bmatrix} \quad \cdots(8)$$

$$\begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = \begin{bmatrix} x'3 \cdot X0 \\ y'3 \cdot Y0 \\ z'3 \cdot Z0 \end{bmatrix} \quad \cdots(9)$$

$$\begin{bmatrix} x \\ y \\ z \end{bmatrix} = \begin{bmatrix} \alpha 11' & \alpha 12' & \alpha 13' \\ \alpha 21' & \alpha 22' & \alpha 23' \\ \alpha 31' & \alpha 32' & \alpha 33' \end{bmatrix} \begin{bmatrix} L-\alpha 14 \\ a-\alpha 24 \\ b-\alpha 34 \end{bmatrix} \quad \cdots(10)$$

However, a^3 expresses cube of a.

[0154] In addition, betaij' (2 i, j= 1, 3) of (8) types is the inverse matrix of betaij (2 i, j= 1, 3) of (2) types. Moreover, alphaij' (i, j= 1, 2, 3, 4) of (10) types is the inverse matrix of alphaij (i, j= 1, 2, 3, 4) of (1) type.

[0155] - The logarithmic transformation machine logarithmic transformation machine 407 changes an RGB code into a MCY signal by the degree type.

$$\left.\begin{array}{l} M1 = -K \cdot \log(G/255) \\ C1 = -K \cdot \log(R/255) \\ Y1 = -K \cdot \log(B/255) \end{array}\right] \quad \cdots(11)$$

However, K whose bottom of a logarithm is 10 is a constant. [0156] The picture signal of M, C, Y, and K is generated in each picture signal generation section by performing masking processing to M1, C1, and Y1 which are outputted here in masking and the UCR section 213.

[0157] Although compression of a picture signal, storage, and expanding were explained above, such actuation is needed because the location of the image formation section of each color has shifted

mutually, as shown in drawing 13. That is, in a certain timing, since the locations of the picture signal which each image formation section needs differ (the locations on an image differ), in order to compensate the time gap, a storage means is used. However, in the case of full color image data, as mentioned above, since the data size is large, by compressing and elongating, the size of image data tends to be decreased and it is going to stop the storage capacity of a needed storage means.

[0158] - the chrominance signal MCYK which generates the decoder which decodes a lightness signal as the total capacity of LUT carried out reduction •••• -- corresponding -- a 4-set individual -- required -- therefore, the LUT -- the object for signals L1 -- four and the object for signals L2 -- four and the object for signal M -- four and the object for signal H -- four -- a total of 16 pieces are needed. The same table is written in these four LUTs. However, since the addresses of LUT accessed since the locations of the picture signal which each image formation section needs differ as mentioned above (the locations on an image differ) differ, respectively, these four LUTs are unrealizable by one ROM etc. simply. Then, as access timing does not collide, it is made to operate in color copying machines 1109 and 1119 by LUT's which divided the usual table's into four equally, i.e., table size's, preparing one fourth of LUTs for each four signals of every, and inputting a signal into each by time sharing as if it was LUT equipped with the usual table.

[0159] Drawing 31 is the block diagram showing the example of a configuration of LUT for decoding a signal L1. In addition, LUT for other signals (L2, M, H) is the same configuration even if data width of face may differ. Moreover, the signal L1 for generating M picture signal is expressed with L1m, and the signal for generating the picture signal of other colors is similarly expressed with L1c, L1y, and L1k below.

[0160] this drawing -- setting -- 501 to 504 -- respectively -- a selector -- it is -- the terminal A of a selector 501 -- signal L1k -- signal L1c is inputted into the terminal A of a selector 503, and signal L1m is inputted into the terminal A of a selector 504 for signal L1y at the terminal A of a selector 502, respectively. 505 to 508 is F/F, respectively and holds the signal inputted from the selector synchronizing with the pixel clock. Since the picture signal is encoded with a 4x4-pixel block as mentioned above, the period for 4 pixels and the inputted signal L1 are held by these F/F and selectors.

[0161] 512 is the selector of 4 input 1 output, and chooses from 509 any of 4 inputs they are according to the selection signal SC mentioned later. A signal L1 is inputted into four input terminals of these selectors in combination different, respectively. Therefore, these selectors will choose the signal L1 which generates the picture signal of a different color. That is, selectors 509-512 are for determining which LUT is accessed to which timing.

[0162] For example, the 9-bit signal L1 is inputted into address terminal AD of 520 from RAM517 through selectors 513-514, respectively, after [which is mentioned later / which was combined with the 2-bit signals HYA, HYB, HYC, and HYD, for example, and became the 11-bit signals LA, LB, LC, and LD] being chosen by selectors 509-512, respectively. In addition, a selector 513 (514,515,516) chooses Signal LA (LB, LC, LD) or an address bus AB according to a selection signal REG.

[0163] 517 to 520 is RAM which constitutes LUT, respectively, and since there is little address width of face by 2 bits compared with a look-up table 1601, storage capacity is set to one fourth. At the time of power-source ON and reset, the table to memorize is downloaded from the control section of the image processing system which is not illustrated with the control signals RAW, RBW, RCW, and RDW made from an address bus AB and a data bus DB, and a chip select and a line signal, and is set up.

[0164] Drawing 32 is the block diagram showing the example of a configuration of the circuit which generates a selection signal SC etc. As shown in this drawing, the value (XPHS-YPHS) which lengthened the output of a subtractor 591, i.e., XPHS to YPHS, is a selection signal SC. Therefore, at the time of YPHS=0, 509 is chosen in order of MCYK ofL1m of selectors, L1c, L1y, and L1k, the order

of KMCY and a selector 511 are chosen, a selector 510 chooses a selector 512 in order of CYMK in order of YKMC similarly, and the signal for generating the same color does not access the same LUT. In addition, it is the same also at the time of YPHS=1, and 2 and 3. Moreover, as shown in this drawing, Signals XSA and XSB should carry out up the AND of the 2 bits of Signal XPHS by NAND gate 575, and are generated, Signal RXP is generated from Signal XPHS and Signals HYA, HYB, HYC, HYD, and RYP are generated from Signal YPHS.

[0165] Drawing 33 is drawing showing an example of the table set as 520 from RAM517, if Signals LA, LB, LC, and LD are 000H altogether at the time of YPHS=0, from RAM517, RA=000H will be outputted and RD=003H from RAM520 will be similarly outputted [RB=001H] for RC=002H from RAM519 from RAM518, respectively. In addition, it is the same also at the time of YPHS=1, and 2 and 3.

[0166] RA, RB, RC, and RD which were outputted from each RAM are the output of a 1-block unit, and sequence is random (see RA, RB, RC, and RD of a showing [in drawing 39]-from drawing 36 timing chart). Then, while returning these signals to 4x4 pixels, it is necessary to double a synchronization. Drawing 34 and 35 are the block diagrams showing the example of circuitry for it.

[0167] The circuit shown in drawing 34 performs the same actuation as the selector 501 and the combination of F/F505 which were shown in drawing 31, and forms the pixel signals NA0-NA3, NB0-NB3, NC0-NC3, and ND0-ND3 (see NA, NB, NC, and ND of the timing chart of drawing 39 from drawing 36) by selector 521-524,533-536,545-548,557-560 and F/F525-532,537-544,549-556,561-564.

[0168] Thus, it inputs into the selectors 565-568 of 16 input 1 output which shows the acquired pixel signals NA0-NA3, NB0-NB3, NC0-NC3, and ND0-ND3 to drawing 35, and random sequence is returned to a right thing. And AO=L1m outputs F/F569, similarly, F/F571 outputs CO=L1y and, as for F/F572, F/F570 outputs DO=L1k for BO=L1c, respectively. At this time, all the values of AO, BO, CO, and DO which are outputted are outputted like ROT-0 of drawing 40. However, the axis of abscissa of 16 measures of this drawing corresponds to XPHS=0, and 1, 2 and 3 (main scanning direction) from the left to the right, respectively, and an axis of ordinate corresponds to YPHS=0, and 1, 2 and 3 (the direction of vertical scanning) from a top to the bottom, respectively.

[0169] In addition, by ****, in order to simplify explanation, the case where Signals LA, LB, LC, and LD were 000H altogether was explained, but even if it is a value different, respectively, the result is the same as the case where it has four LUTs. Moreover, although **** explained only the signal L1, it cannot be overemphasized that other signals L2, M, and H can be similarly processed by LUT of a configuration as mentioned above.

[0170] Thus, although Signal AVE is added to the signals L1, L2, M, and H for generating the picture signal of each obtained color and the lightness signal L is decoded, it is as this configuration having been shown in drawing 16.

[0171] Thus, the color copying machines 1109 and 1119, The same processing information stored in LUT [two or more (n pieces)] is divided into 1/n, and LUT which stored each divided information in n RAM, ROMs, etc. is prepared. To these LUTs usually, in predetermined timing and sequence That is, by inputting the image data encoded by time sharing, parallel processing, such as decode, reverse quantization, etc. for generating two or more color component image data to abbreviation coincidence, is realized. And although the number of LUTs does not change, the sum total of the capacity of the LUT is reduced to the usual 1/n.

[0172] By the way, in ****, only the condition of ROT-0 shown in drawing 40 can be decoded. Then, the output also of the revolution image and mirror image like ROT-1 to ROT-7 which are shown in drawing 40 can be enabled by changing the control signal generation circuit shown in drawing 31 into drawing 41 and the configuration which shows 42.

[0173] For example, when taking ROT-1 (horizontal-scanning vertical scanning is reversed), Signal

ROT is set as '001'=1. Since RTB1= '1' is outputted and others output '0' according to the logical-value table showing a decoder 624 in drawing 43, At the time of YPHS=0, at the time of YPHS=1, Signals HYA, HYB, HYC, and HYD are set to 3, 0, 1, and 2 to 0, 1, 2, and 3, and are set to 1, 2, 3, and 0 to 2, 3, 0, and 1 at the time of YPHS=3 at the time of YPHS=2. Moreover, Signal RXP is set to 3, 2, 1, and 0 corresponding to XPHS=0, and 1, 2 and 3, and Signal RYP is set to 3, 2, 1, and 0 corresponding to YPHS=0, and 1, 2 and 3. Moreover, about a selection signal SC, and XSA and XSB, it is the same as the 1st example.

[0174] A revolution image like ROT-1 shown in drawing 40 can be obtained by inputting these control signals into drawing 31 and the circuit explained by 34 and 35. Moreover, it is possible similarly about ROT-2 to ROT-7 to output a revolution image and a mirror image.

[0175] - Although the data compression section has been explained above a data incompressible system next, explain a data incompressible system.

[0176] Once a data incompressible system goes into the LOG converter 219 shown in drawing 12 (that is, he has no compression) B through the bus selector 222 from the variable power section 208 shown in drawing 12 A and is stored in the incompressible memory 220 through the edge enhancement section 217 from the LOG converter 219 of compression and an incompressible intersection, it is read according to image formation timing, and is sent to the video-processing section 218 of compression and an incompressible intersection through a selector 221.

[0177] Thus, although a compression system and an incompressible system are switched by the bus selector 222 and the selector 221, the select signal is performed by decision of the control section of the image processing system which is not illustrated. That is, mode signal MOD which shows that it is equipped with the DRAM module for incompressible (or DRAM module for compression) is prepared, and a control section judges with which DRAM module it is equipped by this signal MOD. For example, when [which stored image data in the memory section 211, and had a 32M bit address space using the compression system] only the DRAM module with a 2M bit address space is connected, and DRAM module connection is made, image data is stored in the incompressible memory 220 using an incompressible system.

[0178] - Explain the case where a multiple-value image is inputted, from an external input system, next the exterior of color copying machines 1109 and 1119.

[0179] Like [after going into the color space compression zone 207 through the bus selector 232] the above-mentioned, once the image data of 8 bits each of RGB inputted from external I/F231 shown in drawing 12 A is stored in the memory section 211 or the incompressible memory 220, it is read according to image formation timing, and is sent to the video-processing section 218.

[0180] If RGB 3 color is simultaneously inputted from the outside at this time, it is also possible to be also able to store in the incompressible memory 220, without compressing as it is, to compress, and to store in the memory section 211. However, since picture compression using Lab space cannot be performed unless it is 3 color coincidence when image data is inputted by Junji Men of RGB (or CMY (K)) from the exterior, it is necessary to store the image data for every color in the incompressible memory 220 in each image generation section 233 one by one. Therefore, image data is unstorable unless it is equipped [that is,] with the DRAM module with a 32M bit address space without the incompressible memory 220, when image data is inputted into Junji Men from the exterior.

[0181] - Explain the case where a binary picture is inputted, from the exterior of binary picture data, next color copying machines 1109 and 1119.

[0182] As well as the case of a multiple-value image when binary picture data are inputted by Junji Men of RGB (or CMY (K)) using the least significant bit (LSB) of external I/F231, it stores in memory, after changing into multiple-value data using a serial-parallel transducer as shows an example to drawing 44, just before inputting into memory. For example, also by the image information of A3 size, if 1 bit of binary data is changed into 16 bits, as shown in drawing 27, storing will become possible in

a 21-bit address space. Moreover, it returns to the original binary data immediately after reading from memory using a parallel serial conversion machine as shows an example to drawing 45. furthermore, the least significant bit (LSB) of image data -- '0' -- if it becomes -- '00H' -- outputting -- '1' -- if the gamma correction section 215 is set up so that 'FFH' may be outputted, if it becomes, the output of a binary picture is also possible.

[0183] - Explain a control unit, next the control unit of color copying machines 1109 and 1119.

[0184] Drawing 46 is drawing showing the example of a configuration of a control unit, 2401 is a ten key, 2402 is a reset key, and an operator performs setting out of operation and reset of a copying machine using these keys. 2403 is a copy start key and a copying machine starts copy actuation by depressing this. 2404 is display units, such as liquid crystal, and has the display and the touch panel key made to correspond. The control section of the image processing system which is not illustrated deals with the key input from a touch panel, and the key input from hardkeys, such as a ten key 2401 and the copy start key 2403, fair. 2405 is an example of a display on the display unit 2404. 2406 is a remote key, and in the case of the local mode using color copying machines 1109 and 1119, it turns off alone, and, in the case of the remote state which inputs image data from the exterior, turns on.

[0185] The case where JPEG data are inputted into [the interface of JPEG data], next color copying machines 1109 and 1119 is explained.

[0186] Drawing 47 is the block diagram showing the example of a configuration which added the JPEG data-processing section to the configuration of the image processing system explained by drawing 12 A, and when JPEG data have been sent to the color copying machine 1119 through a color copying machine 1109 or a server 1117 from the ATM network 1101, JPEG data are inputted through JPEG-I/F241. Once the JPEG data inputted into JPEG-I/F241 are stored in the page memory 242, they are read from the page memory 242 synchronizing with image formation timing, and are decoded in the procedure mentioned above in the JPEG expanding section 243 equipped with the configuration shown in drawing 4.

[0187] On the other hand, the control section of the image-processing section which is not illustrated sends out a select signal to the bus selector 232 based on the signal which shows that the image data sent from the interface sections, such as external I/F231 and JPEG-I/F241, was received. The image data changed and decoded so that the bus selector 232 might choose the data from the JPEG data-processing section is sent to the video-processing section 218 through the color space compression zone 207, the variable power section 208, the bus selector 222, --, the edge enhancement section 217 and a selector 221 by this select signal. That is, it does not pass along a compression system and the incompressible memory 220.

[0188] Here, it is because JPEG data are variable length to store JPEG data in the page memory 242 once. That is, the image processing system of copying machines 1109 and 1119 needs to output image data at the always same speed, and uses the page memory 242 for the speed conversion for it. Therefore, the writing to the page memory 242 is performed at a JPEG data transfer rate, and read-out is performed by the output rate of the printer section 103.

[0189] Drawing 48 to drawing 50 is drawing explaining an example of R/W control of the page memory 242.

[0190] In drawing 48, when variable-length JPEG data have been sent in order of A, B, C, D, and -- from JPEG-I/F241, the one address (however, in the case of DRAM, it is regarded as the one address by the row address and the column address) and WE signal are generated to the data for one scan. That is, when JPEG data are assembled by one scan, as shown in drawing 49, JPEG data are once written in the addresses A, B, C, and D with which it continued on the page memory 242, and the order transmitted to --, using 8x8 pixels as 1 block. That is, JPEG data will be written in the page memory 242 asynchronous.

[0191] Then, after a JPEG data transfer is all completed, as shown in drawing 50, read-out of JPEG

data is performed synchronizing with image formation timing. That is, the one address and RE signal are generated using 8x8 pixels as 1 block, according to it, reading appearance is carried out, it is restored to 8x8-pixel image data in the JPEG expanding section 243, and JPEG data are sent to the bus selector 232.

[0192] In addition, if the interface equipped with the decoder as shown not only in JPEG-I/F but in drawing 8 is prepared for color copying machines 1109 and 1119, MPEG data can be received to them and the printed output of the request frame can also be carried out to them.

[0193] [State transition of image processing system] drawing 52 is drawing explaining the example of a state transition of the image processing system shown in drawing 47, and is performed by the control section of the image processing system which is not illustrated.

[0194] In this drawing, if a power source is switched on in the condition S1, it changes to a condition S2 and will be in a system initialization condition, and initialization of the system containing an image processing system is performed.

[0195] Next, when the remote key 2406 of a control unit is OFF, or when a remote state is canceled in the remote idle state S5 mentioned later, local assignment is carried out, and it is •••••• to the local idle state S3. If a start key 2403 is pushed at this time, it will change to local busy condition S4, and copy actuation will be started. And after copy actuation is completed, it returns to the local idle state S3 again, and stands by.

[0196] Moreover, when the remote key 2406 is ON, or when a remote state is set up in the local idle state S3, remote assignment is carried out, and it changes to the remote idle state S5. If a command is inputted from a host machine (for example, personal computer 1115) etc. at this time, it will change to the remote busy condition S6, and JPEG data and RGB data which have been sent to JPEG-I/F241 or external I/F231 will be processed according to that command. And it returns to the remote idle state S6 again after command termination, and stands by.

[0197] In addition, when it is [be / it / under / transition / including] in local busy condition S4, while forbidding the input of JPEG-I/F241 or external I/F231, the command inputted from a host machine etc. is made into an invalid. When it is [be / it / under / transition / including] in the remote busy condition S6, while similarly forbidding copy actuation, the input from the copy start key 2403 etc. is made into an invalid.

[0198] Image data which read the manuscript image by which a synchronous input is carried out according to this example as explained above, The ATM network which carries out the ATM transfer of the image data encoded by various methods, such as JPEG and MPEG, Or the image data by which an asynchronous input is carried out from LAN using the Ethernet transmitted in the modes other than ATM By storing variable-length code data in memory once, changing a transfer timing or a transfer frequency and carrying out an image output, when outputting with the same image processing systems (color copying machine which outputs an image with constant speed) It enables the image data by which the synchronous input was carried out, and the image data by which the asynchronous input was carried out from the network to carry out a high-speed output with constant speed. Moreover, even when the image data by which variable length coding was carried out is inputted to the image processing system equipped with two or more image formation sections which were mentioned above, it becomes possible to double the formation timing of each color.

[0199]

[The 2nd example] Hereafter, the image processing system of the 2nd example concerning this invention is explained. In addition, in the 2nd example, about the same configuration as the 1st example and abbreviation, the same sign is attached and the detail explanation is omitted.

[0200] In the 1st example, although JPEG data are once stored in the page memory 242, since the page memory 242 of big memory size is needed in this case, the 2nd example makes the transfer rate conversion by this page memory 242 serve a double purpose in the memory section 211.

[0201] That is, after compressing JPEG considering 8x8 pixels as 1 block and carrying out sequential decoding of them, the image data of the pixel unit which decoded for eight lines which is block width of face at least is held, it is an image clock quick enough, and if those data are read, it will become possible serially to develop to the image data of a pixel unit.

[0202] Drawing 51 is the block diagram showing the example of a configuration of the JPEG data-processing section of the 2nd example, prepares the buffer memory 244 holding the image data for at least eight lines outputted from the JPEG expanding section 243, and reads image data with an image clock quick enough. Next, bus selector 232 Image data is changed, compression processing which mentioned above again the image data which read the manuscript, and the image data which elongated the received JPEG data in the compression zone 210 through the color space compression zone 207 and the variable power section 208 in common is performed, and it stores in the memory section 211. However, in the image processing system equipped with two or more image formation sections, in order to double the phase of each color, memory is required for performing such picture compression, and it is for reducing the huge memory size. When all image data is compressed and stored, according to the rate of the printer section 103, data are read from the memory section 211. Since it is the same procedure as the 1st example henceforth, explanation is omitted.

[0203] In addition, even if it applies this invention to the system which consists of two or more devices, it may be applied to the equipment which consists of one device.

[0204] Moreover, it cannot be overemphasized that this invention can be applied also when attained by supplying a program to a system or equipment.

[0205]

[Effect of the Invention] As explained above, according to this invention, the image processing system, the image-processing approach, and network system which reduce memory size using a common coding means can be offered irrespective of the inputted image data.

[Translation done.]

• NOTICES •

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TECHNICAL FIELD

[Industrial Application] This invention relates to the image processing system which processes and outputs the inputted image data, the image-processing approach, and the network system which connected the image processing system, concerning an image processing system, the image-processing approach, and a network system.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] The image data whose color was separated is treated, it connects with the Local Area Network (henceforth "LAN") using the ATM network transmitted by ATM (Asynchronous Transfer Mode), or the Ethernet which transmits data in the modes other than ATM, and the interface of an image processing system transmits or outputs the image data encoded by coding methods, such as JPEG and MPEG. However, a limping gait, such as changing and outputting the image data itself whose color was separated, and the data which encoded them, is not.

[Translation done.]

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, there were the following troubles in the above-mentioned conventional example. The image processing system itself needs to output image data with constant speed. In the equipment especially equipped with two or more image formation means, unless image data is outputted with constant speed from an image-processing means, an image cannot be formed. That is, when there are image data which read the manuscript image by which a synchronous input is carried out, and image data to which variable length coding inputted through an ATM network, such as JPEG and MPEG, was given, an image processing system must output both image data with constant speed.
[0004] Furthermore, in the image processing system equipped with the image memory, in order to reduce the memory size, the approach of compressing into the image memorized to an image memory is taken. However, the image processing system which performs such picture compression is not taken into consideration to being used combining a network system which was mentioned above.
[0005] This invention aims at offering the image processing system, the image-processing approach, and network system for solving an above-mentioned problem which can reduce memory size using a coding means common irrespective of the image data which it is and was inputted.

[Translation done.]

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[0005] This invention aims at offering the image processing system, the image-processing approach, and network system for solving an above-mentioned problem which can reduce memory size using a coding means common irrespective of the image data which it is and was inputted.

[Translation done.]